

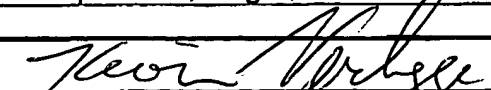
Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 042P8931C	Application Number: 10/620,629
Sheet 2 of 4		First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
		Filing Date: July 15, 2003	Art Unit: 2188
OTHER ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
KW	A08	AGARWAL, A., et al., "The MIT Alewife Machine: A Large-Scale Distributed-memory Multiprocessor," <i>Technical Report MIT/LCS Memo TM-454, Laboratory for Computer Science, Massachusetts Institute of Technology</i> , 1991.	
KW	A19	ANDERSON, C., et al., "A Multi-Level Hierarchical Cache Coherence Protocol for Multiprocessors," <i>University of Washington</i> , 1992, 92-10-04	
KW	A18	ANDERSON, C., et al., "Design and Evaluation of a Subblock Cache Coherence Protocol for Bus-Based Multiprocessors," <i>University of Washington</i> , 1994, 94-05-02	
KW	A09	BIANCHI, R., et al., "Memory Contention in Scalable Cache-coherent Multiprocessors," <i>Technical Report 448, Computer Science Department, University of Rochester</i> , 1993.	
KW	B01	CENSIER, L.M., et al., "A New Solution to Coherence Problems in Multicache Systems," <i>IEEE Transactions on Computers</i> , Vol. C-27, No. 12, December, 1978, 7 pages	
KW	A20	CHAIKEN, D., et al., "LimitLESS Directories: A Scalable Cache Coherence Scheme," <i>Proceedings of the 4th Int'l Conference on ASPLOS</i> , pages 224-234, New York, April 1991.	
KW	A22	EGGERS, S.J., et al., "A Characterization of Sharing in Parallel Programs and Its Application to Coherency Protocol Evaluation," <i>Proceedings of the 15th Annual International Symposium on Computer Architecture</i> , May 1988.	
KW	A10	FARKAS, K., "Cache Consistency in Hierarchical-ring-based Multiprocessors," <i>Technical Report CSRI-273, Computer Systems Research Institute, University of Toronto, Ontario, Canada</i> , January 1993.	
KW	A11	FLEISCH, B., "A Coherent Distributed Shared Memory Design," <i>Proceedings from the 14th ACM Symposium on Operating System Principles</i> , pages 211-223, New York, 1989.	

Examiner Signature	<i>Kevin Verbrugge</i>	Date Considered	8/19/05
-----------------------	------------------------	--------------------	---------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 042P8931C	Application Number: 10/620,629
Sheet 3 of 4		First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
		Filing Date: July 15, 2003	Art Unit: 2188
OTHER ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
KW	A06	GHARACHORLOO, K., et al., "Memory Consistency and Event Ordering in Scalable Shared-Memory Multiprocessors," <i>Proceedings of the 17th International Symposium on Computer Architecture</i> , pages 15-26, May 1990.	
KW	A05	GHARACHORLOO, K., et al., "Performance Evaluation of Memory Consistency Models for Shared-Memory Multiprocessors," <i>Proceedings of Fourth International Conference on Architectural Support for Programming Languages and Operating Systems</i> , pages 245-257, 1991.	
KW	A03	IEEE Std 1596-1992. "Scalable Coherent Interface," Piscataway, NJ.	
KW	A04	JOHNSON, R.E., "Extending the Scalable Coherent Interface for Large-Scale Shared-Memory Multiprocessors," <i>PhD Thesis, University of Wisconsin-Madison</i> , 1993.	
KW	A23	LENOSKI, D., et al., "The Directory-based Cache Coherence Protocol for the Dash Multiprocessor," <i>Proceedings of the 17th Int'l Symposium on Computer Architecture</i> , Los Alamitos, Calif., May 1990.	
KW	A13	LI, K., et al., "Memory Coherence in Shared Virtual Memory Systems," <i>ACM Transactions On Computer Systems</i> , 7(4):321-359, November 1989.	
KW	A14	LI, Q., et al., "Redundant Linked List based Cache Coherence Protocol," <i>World Computer Congress, IFIP Congress</i> , 1994.	
KW	A01	LILJA, D. J., "Cache Coherence in Large-Scale Shared-Memory Multiprocessors: Issues and Comparisons," <i>ACM Computing Surveys</i> , 25(3), September 1993	
KW	A15	MELLOR-CRUMMEY, J.M., et al., "Algorithms for Scalable Synchronization on Shared-memory Multiprocessors," <i>ACM Transactions on Computer Systems</i> , 9(1), Feb 1991.	
KW	A12	MORI, S., et al., "A Distributed Shared Memory Multiprocessor: ASURA - Memory and Cache Architectures," <i>Supercomputing '93</i> , pages 740-749, Portland, Oregon, November 1993.	
Examiner Signature			Date Considered 8/19/05

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 042P8931C	Application Number: 10/620,629
Sheet 4 of 4		First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
		Filing Date: July 15, 2003	Art Unit: 2188
OTHER ART - NON PATENT LITERATURE DOCUMENTS			
KW	A16	NILSSON, H., et al., "The Scalable Tree Protocol - a Cache Coherence Approach to Large-scale Multiprocessors," <i>Proceedings of the 4th IEEE Symposium on Parallel and Distributed Processing</i> , May 1992.	
KW	A24	NITZBERG, B., et al., "Distributed Shared Memory: A Survey of Issues and Algorithms," <i>IEEE Computer</i> , pages 52-60, August 1991.	
KW	A02	PAPAMARCOS, M., et al., "A Low-Overhead Coherence Solution for Multiprocessors with Private Cache Memories," <i>Proc. 11th ISCA</i> , 1984, pp. 348-354.	
KW	B03	PCT International Search Report, PCT/US01/30359, mailed 10/08/2002, 5 pages	
KW	B02	PONG, F., et al., "Correctness of a Directory-Based Cache Coherence Protocol: Early Experience," <i>IEEE</i> , 1993, pp. 37-44	
KW	A21	SANDHU, H.S., et al., "The Shared Regions Approach to Software Cache Coherence on Multiprocessors," <i>Proceedings of the 4th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming</i> , May 1993.	
KW	A07	SCHEURICH, C., et al., "Correct Memory Operation of Cache-Based Multiprocessors," <i>Proceedings 14th Annual International Symposium on Computer Architecture</i> , pages 234-243, Pittsburgh, PA, June 1987.	
KW	A25	STUMM, M., et al., "Algorithms Implementing Distributed Shared Memory," <i>Computer</i> , 23(5):54-64, May 1990.	
KW	A17	TANG, C.K., "Cache System Design in the Tightly Coupled Multiprocessor System," <i>AFIPS Proceedings of the National Computer Conference</i> , 1976.	
KW	A27	THAKKAR, S., et al., "Scalable Shared-Memory Multiprocessor Architectures," <i>IEEE Computer</i> , 23(6), June 1990.	
KW	A26	THAPAR, M., et al., "Stanford Distributed Directory Protocol," <i>IEEE Computer</i> , pages 78-80, June 1990.	
KW	C01	Patent Act 1977: Examination Report under section 18(3), Application No: GB0309110.5 (International App. No. PCT/US01/30359), July 7, 2004	

Examiner Signature		Date Considered	8/18/05
-----------------------	---	--------------------	---------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

†Unique citation designation number. *Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.